<u>Claims</u>

1.   (Previously presented) A computer-implemented method, comprising:

inputting a netlist;

generating symbols and connections formed according to the netlist and at least in part

according to connectivity strength between at least a first symbol and a second symbol, the first

symbol and the second symbol having at least one connection between the first symbol and the

second symbol, the connectivity strength corresponding to a quantification of the at least one

connection between the first symbol and the second symbol; and

generating a wiring harness diagram that comprises the symbols and the connections.

2.   (Previously presented) The method of claim 1 in which generating the wiring

harness diagram comprises sorting the netlist at least in part according to the connectivity

strength.

3.   (Previously presented) A computer-implemented method, comprising:

inputting a netlist;

generating symbols and connections formed according to the netlist; and

generating a wiring harness diagram, wherein the wiring harness diagram comprises the

symbols and the connections, and wherein generating the wiring harness diagram comprises

positioning a pin on a side of a first symbol, the side selected according to a connectivity strength

corresponding to the number of connections between the first symbol and a second symbol.

4.   (Previously presented) The method of claim 1 further comprising:

sequencing symbol placement for the wiring harness diagram such that symbols with

predetermined pin positions are placed in the wiring harness diagram with higher priority than

symbols for which the side of the symbol for placing a pin may be selected.

5.   (Previously presented) A computer-implemented method, comprising:

sequencing symbol placement in a wiring harness layout at least in part according to the

connectivity strength of at least one pair of symbols, wherein the connectivity strength

corresponds to a number of connections existing between the at least one pair of symbols, the

number of connections existing between the at least one pair of symbols being one or more; and

generating a wiring harness diagram for at least one bundle according to the wiring

harness layout, wherein the bundle comprises a plurality of wires.

6.   (Original) The method of claim 5 further comprising:

selecting a side of a first symbol on which to position a pin to increase the directness of

connectivity between the first symbol and a second symbol.

7.   (Original) The method of claim 5 in which generating a wiring diagram according

to the layout further comprises:

selecting sides of the symbols on which to position pins according to a selected layout

dimension; and

arranging the pins on the selected sides to increase the directness of connections between

the symbols.

8.   (Original) The method of claim 5 further comprising:

sequencing symbol placement for the wiring harness diagram such that symbols with

predetermined pin positions are placed in the layout with higher priority than symbols for which

the side of the symbol for placing a pin may be selected.

9.   (Previously presented) A computer-implemented method, comprising:

sequencing symbol placement in a wiring harness layout for at least one bundle

comprising signal-carriers, at least in part according to the connectivity strength of at least one

pair of symbols, the at least one pair of symbols having at least one connection in-between, the

connectivity strength being determined by the at least one connection in-between the at least one

pair of symbols; and

selecting a side of a first symbol on which to place a pin to increase the directness of

connectivity between the first symbol and a second symbol.

10.   (Original) The method of claim 9 in which selecting the side of the first symbol

further comprises:

selecting the side according to a selected layout dimension and a position of the second

symbol.

11.   (Previously presented) The method of claim 9 further comprising:

sequencing symbol placement for the wiring harness layout such that symbols with

predefined pin positions are placed in the layout with higher priority than symbols for which the

side of the symbol for placing a pin may be selected.

12.   (Previously presented) A computer-implemented method, comprising:

when at least one first pair of symbols of a netlist has been placed in a wiring harness

layout, selecting a next pair of symbols to place in the layout comprising at least one symbol of

the first pair; and

when there is at least one predefined symbol in the netlist, selecting as the next pair of

symbols a pair of symbols having the largest number of connections and comprising a predefined

symbol.

13.   (Original) The method of claim 12 further comprising:

selecting for the placement of pins a side of one symbol of the next pair of symbols; and

arranging the pins along the side to increase the directness of connection between the

next pair of symbols.

14.   (Previously presented) An article comprising:

a machine-readable media comprising instructions which, when executed by the

processor of a data processing device, result in:

inputting a netlist;

generating symbols and connections formed according to the netlist and at least in part

according to connectivity strength between at least a first symbol and a second symbol, the first

symbol and the second symbol having at least one connection between the first symbol and the

second symbol, the connectivity strength corresponding to a quantification of the at least one

connection between the first symbol and the second symbol; and

generating a wiring harness diagram that comprises the symbols and the connections.

15.   (Previously presented) The article of claim 14 in which the instructions, when

executed by the processor to generate the wiring harness diagram, further result in:

sorting the netlist at least in part according to the connectivity strength.

16.   (Previously presented) The article of claim 14 in which the instructions, when

executed by the processor to generate the symbols, further result in:

positioning a pin on a side of the first symbol, the side selected according to a connection

between the first symbol and the second symbol.

17.   (Previously presented) The article of claim 14 in which the instructions, when executed by the processor, further result in:

sequencing symbol placement for the wiring harness diagram such that symbols with predetermined pin positions are placed in the wiring harness diagram with higher priority than symbols for which the side of the symbol for placing a pin may be selected.

18.   (Previously presented) An article comprising:

a machine-readable media comprising instructions which, when executed by the processor of a data processing device, result in:

sequencing symbol placement in a wiring harness layout at least in part according to the connectivity strength of at least one pair of symbols, wherein the connectivity strength corresponds to a number of connections existing between the at least one pair of symbols, the number of connections existing between the at least one pair of symbols being one or more; and

generating a wiring harness diagram for at least one bundle according to the wiring harness layout, wherein the bundle comprises a plurality of wires.

19.   (Previously presented) The article of claim 18 in which the instructions, when executed by the processor, further result in:

selecting a side of a first symbol on which to position a pin to increase the directness of connectivity between the first symbol and a second symbol.

20.   (Previously presented) The article of claim 18 in which the instructions, when

executed by the processor to generate the wiring harness diagram, further result in:

selecting sides of the symbols on which to position pins according to a selected layout

dimension.

21.   (Previously presented) The article of claim 18 in which the instructions, when

executed by the processor, further result in:

sequencing symbol placement for the wiring harness diagram such that symbols with

predetermined pin positions are placed in the layout with higher priority than symbols for which

the side of the symbol for placing a pin may be selected.

22.   (Previously presented) An article comprising:

a machine-readable media comprising instructions which, when executed by the

processor of a data processing device, result in:

sequencing symbol placement in a wiring harness layout for at least one bundle

comprising signal-carriers, at least in part according to the connectivity strength of at least one

pair of symbols, the at least one pair of symbols having at least one connection in-between, the

connectivity strength being determined by the at least one connection in-between the at least one

pair of symbols; and

selecting a side of a first symbol on which to place a pin to increase the directness of

connectivity between the first symbol and a second symbol.

23.   (Previously presented) The article of claim 18 in which the instructions, when

executed by the processor to select the side of the first symbol, further result in:

selecting the side according to a selected wiring harness layout dimension and a position

of the second symbol.

24.   (Previously presented) The article of claim 22 in which the instructions, when

executed by the processor, further result in:

sequencing symbol placement for the wiring harness layout such that symbols with

predefined pin positions are placed in the layout with higher priority than symbols for which the

side of the symbol for placing a pin may be selected.

25.   (Previously presented) An article comprising:

a machine-readable media comprising instructions which, when executed by the

processor of a data processing device, result in:

when at least one first pair of symbols of a netlist has been placed in a wiring harness

layout, selecting a next pair of symbols to place in the layout comprising at least one symbol of

the first pair; and

when there is at least one predefined symbol in the netlist, selecting as the next pair of

symbols a pair of symbols having the largest number of connections and comprising a predefined

symbol.

26.   (Previously presented) The article of claim 25 in which the instructions, when executed by the processor, further result in:

selecting for the placement of pins a side of one symbol of the next pair of symbols.

27.   (Previously presented) An apparatus comprising:

a processor; and

a machine-readable media comprising instructions which, when executed by the processor, result in:

inputting a netlist;

generating symbols and connections formed according to the netlist and at least in part according to connectivity strength between at least a first symbol and a second symbol, the first symbol and the second symbol having at least one connection between the first symbol and the second symbol, the connectivity strength corresponding to a quantification of the at least one connection between the first symbol and the second symbol; and

generating a wiring harness diagram that comprises the symbols and the connections.

28.   (Previously presented) The apparatus of claim 27 in which the instructions, when executed by the processor to generate the wiring harness diagram, further result in:

sorting the netlist at least in part according to the connectivity strength.

29.   (Previously presented) The apparatus of claim 27 in which the instructions, when executed by the processor to generate the symbols, further result in:

positioning a pin on a side of the first symbol, the side selected according to a connection between the first symbol and the second symbol.

30.   (Original) The apparatus of claim 27 in which the instructions, when executed by the processor, further result in:

sequencing symbol placement for the wiring harness layout such that symbols with predetermined pin positions are placed in the wiring harness diagram with higher priority than symbols for which the side of the symbol for placing a pin may be selected.

31.   (Previously presented) An apparatus comprising:

a processor; and

a machine-readable media comprising instructions which, when executed by the processor, result in:

sequencing symbol placement in a wiring harness layout at least in part according to the connectivity strength of at least one pair of symbols, wherein the connectivity strength corresponds to a number of connections existing between the at least one pair of symbols, the number of connections existing between the at least one pair of symbols being one or more; and

generating a wiring harness diagram for at least one bundle according to the wiring harness layout, wherein the bundle comprises a plurality of wires.

32.   (Original) The apparatus of claim 31 in which the instructions, when executed by

the processor, further result in:

selecting a side of a first symbol on which to position a pin to increase the directness of

connectivity between the first symbol and a second symbol.

33.   (Original) The apparatus of claim 32 in which the instructions, when executed by

the processor to generate the wiring harness diagram, result in:

selecting sides of the symbols on which to position pins according to a selected layout

dimension; and

arranging the pins on the sides to increase the directness of connection between the

symbols.

34.   (Original) The apparatus of claim 32 in which the instructions, when executed by

the processor, further result in:

sequencing symbol placement for the wiring harness layout such that symbols with

predetermined pin positions are placed in the layout with higher priority than symbols for which

the side of the symbol for placing a pin may be selected.

35.   (Previously presented) An apparatus comprising:

a processor; and

a machine-readable media comprising instructions which, when executed by the

processor, result in:

sequencing symbol placement in a wiring harness layout for at least one bundle

comprising signal-carriers, at least in part according to the connectivity strength of at least one

pair of symbols, the at least one pair of symbols having at least one connection in-between, the

connectivity strength being determined by the at least one connection in-between the at least one

pair of symbols; and

selecting a side of a first symbol on which to place a pin to increase the directness of

connectivity between the first symbol and a second symbol.

36.   (Original) The apparatus of claim 35 in which the instructions, when executed by

the processor to select the side of the first symbol, result in:

selecting the side according to a selected layout dimension and a position of the second

symbol.

37.   (Original) The apparatus of claim 35 in which the instructions, when executed by

the processor, further result in:

sequencing symbol placement for the layout such that symbols with predefined pin

positions are placed in the layout with higher priority than symbols for which the side of the

symbol for placing a pin may be selected.

38.   (Previously presented) An apparatus comprising:

a processor; and

a machine-readable media comprising instructions which, when executed by the

processor, result in:

when at least one first pair of symbols of a netlist has been placed in a wiring harness

layout, selecting a next pair of symbols to place in the layout comprising at least one symbol of

the first pair; and

when there is at least one predefined symbol in the netlist, selecting as the next pair of

symbols a pair of symbols having the largest number of connections and comprising a predefined

symbol.

39.   (Original) The apparatus of claim 38 in which the instructions, when executed by

the processor, further result in:

selecting for the placement of pins a side of one symbol of the next pair of symbols.

40.   (Previously presented) A carrier wave, comprising:

signals defining component symbols and connections generated according to a netlist and

a selected wiring harness layout dimension and at least in part according to a connectivity

strength between a first symbol and a second symbol, the symbols and connections defining a

wiring harness diagram along the layout dimension.

41.   (Previously presented) A carrier wave, comprising:

signals defining a first and second component symbols, the component symbols

comprising pins, the pins positioned on sides of the symbols selected to increase the directness of

connectivity between the first symbol and the second symbol, the connectivity corresponding to

the quantization of connections between the first symbol and the second symbol.

42.   (Previously presented) The method of claim 1, wherein the wiring harness

diagram corresponds to a wiring harness, the wiring harness comprising at least one bundle of

signal-carrying wires.

43.   (Previously presented) The method of claim 1, wherein the wiring harness

diagram is generated along a selected wiring harness layout dimension.

44.   (Previously presented) The method of claim 42, wherein the signal-carrying wires

carry electrical signals.

45.   (Previously presented) The method of claim 42, wherein the signal-carrying wires

carry optical signals.

46.   (Previously presented) The method of claim 1, wherein the wiring harness

diagram represents a wiring harness that establishes connectivity between at least two

components.

47.   (Previously presented) The method of claim 46, wherein at least one component is an electrical component.

48.   (Previously presented) The method of claim 46, wherein at least one component is an optical component.

49.   (Previously presented) The method of claim 1, wherein the act of generating a wiring harness diagram comprises resizing at least one symbol.

50.   (Previously presented) The method of claim 1, wherein the act of generating a wiring harness diagram comprises repositioning at least one symbol.

51.   (Previously presented) The method of claim 1, wherein the wiring harness diagram further comprises pins, wherein the act of generating the wiring harness diagram comprises arranging the pins to increase directness of connections between at least two symbols, and wherein at least one symbol is resized and at least one symbol is repositioned.

52.   (Previously presented) The method of claim 7, wherein arranging the pins comprises resizing at least one symbol.

53.   (Previously presented) The method of claim 7, wherein arranging the pins comprises repositioning at least one symbol.